REMARKS

Claims 46-48, 51-56, 58-60, 62-65 and 67-74 and 76-91 are pending in this application. Claim 76 has been amended. No new matter has been introduced.

Claims 46, 51, 52, 54, 56, 58 and 59 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Asakawa et al. (U.S. Patent No. 5,565,607) ("Asakawa"). This rejection is respectfully traversed.

The claimed invention relates to semiconductor devices and, in particular, to buried conductors within a substrate. As such, independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Independent claim 46 also recites that the buried conductor pattern "is completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate." Independent claim 46 further recites "a conductive path extending from said buried conductor pattern to said devices."

Independent claim 56 recites a buried conductor pattern within a "monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein." Independent claim 56 also recites "a conductive material filling said empty space pattern such that said conductive material is below a top surface of said monocrystalline substrate and forms a buried conductor pattern, said buried conductor pattern being completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate." Independent claim 56 further recites "a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate."

Asakawa relates to a "semiconductor substrate" that "comprises a foundation, a semiconductor monocrystalline film formed on the foundation, and a high-melting-point metal film or a high-melting-point metal alloy film disposed in at least part of a region between the semiconductor monocrystalline film and the foundation." (Abstract). Asakawa also teaches that "[T]he high-melting-point metal film disposed below the semiconductor monocrystalline film can be utilized as a conductor in a semiconductor device." (Abstract).

Asakawa does not anticipate the subject matter of claims 46, 51, 52, 54, 56, 58 and 59. Asakawa does not disclose, teach or suggest a buried conductor pattern that is "completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as independent claims 46 and 65 recite. Asakawa teaches that tungsten film 5 is formed over silicon oxide film 4 and that monocrystalline silicon film 14 is subsequently formed over the tungsten film 5. (Col. 3, lines 24-36). However, no structure in Asakawa is a buried conductor pattern "*completely surrounded* by the same monocrystalline substrate material of a same conductivity type," as in the claimed invention (emphasis added). For at least these reasons, Asakawa fails to anticipate the subject matter of claims 46, 51, 52, 54, 56, 58 and 59, and withdrawal of the rejection of these claims is respectfully requested.

Claims 47, 48, 72, 73, 76-79 and 81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakawa in view of Kenney (U.S. Patent No. 5,583,368). This rejection is respectfully traversed.

As noted, independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Independent claim 46 also recites that the buried conductor pattern "is

completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate."

Independent claim 72 recites an "integrated circuit substrate comprising a plurality of buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate." Independent claim 72 also recites that the buried conductor patterns form "at least a part of an interconnect between devices."

Amended independent claim 76 recites an "integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline material of a same conductivity type of said monocystalline substrate." Amended independent claim 76 also recites that the first and second buried conductive patterns form "at least a part of first and second interconnects between devices, respectively, wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate."

Kenney relates to "[c]hips having subsurface structures within or adjacent a horizontal trench in bulk single crystal semiconductor." (Abstract). According to Kenney, "[s]tructures include three terminal devices, such as FETs and bipolar transistors, rectifying contacts, such as pn diodes and Schottky diodes, capacitors, and contacts to and connectors between devices." (Abstract). Kenney also teaches a "process for forming a horizontal trench exclusively in heavily doped p+ regions is

presented in which porous silicon is first formed in the p+ regions and then the porous silicon is etched." (Abstract).

The subject matter of claims 47, 48, 72, 73, 76-79 and 81 would not have been obvious over Asakawa and Kenney. Specifically, the October 19, 2005 Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, Asakawa and Kenney, considered alone or in combination, fail to disclose, teach or suggest all limitations of independent claims 46, 72 and 76. Neither Asakawa nor Kenney teaches or suggests a "buried conductor pattern . . . *completely surrounded* by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as independent claim 46 recites (emphasis added). The cited references, alone or in combination, also fail to disclose, teach or suggest "a plurality of buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are *completely surrounded* by the same monocrystalline substrate material of said monocrystalline substrate," as independent claim 72 recites (emphasis added).

Moreover, none of Asakawa and Kenney teaches or suggests "first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductors pattern is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate," and "*completely surrounded* by the same monocrystalline material of a same conductivity type of said monocystalline substrate," as independent claim 76 recites (emphasis added). For at least these reasons, the subject matter of claims 47, 48, 72, 73, 76-79 and 81 would not have been obvious over Asakawa and Kenney, and withdrawal of the rejection of these claims is respectfully requested.

Claim 53 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakawa in view of Witek et al. (U.S. Patent No. 5,291,438) ("Witek"). Claim 55 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakawa in view of Choi (U.S. Patent No. 6,215,158) ("Choi"). Claim 60 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakaawa and further in view of Sato et al., *A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) Induced by Silicon Surface Migration*, 1999 IEEE, pp. 517-20 ("Sato"). These rejections are respectfully traversed.

Claims 53 and 55 depend on independent claim 46. Claim 60 depends on independent claim 56. As noted above, Asakawa fails to disclose, teach or suggest all limitations of independent claims 46 and 56. In addition, Witek, Choi and Sato fail to supplement the deficiencies of Asakawa. For at least these reasons, withdrawal of the rejection of claims 53, 55 and 60 is also respectfully requested.

Claims 62-64 and 67-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakawa in view of Tsu et al. (U.S. Patent No. 6,294,420 B1) ("Tsu"). This rejection is respectfully traversed.

Independent claim 62 recites "a processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein." Independent claim 62 also recites "a conductive material filling said empty space pattern such that said conductive material is below a top surface of said monocrystalline substrate and said conductive structure is completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate."

Tsu relates to "an integrated circuit capacitor and a method of forming a capacitor." (Col. 1, lines 14-15). Tsu discloses that a capacitor may be used in a DRAM array, and that the memory array may be "embedded in a larger integrated circuit device." (Col. 7, lines 54-62; Col. 8, lines 61-67).

The subject matter of claims 62-64 and 67-71 would not have been obvious over Asakawa and Tsu. Again, the Office Action fails to establish a *prima facie* case of obviousness. None of Asakawa and Tsu, considered alone or in combination, discloses, teaches or suggests all limitations of independent claim 62. Asakawa and Tsu fail to teach or suggest a "processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein," as independent claim 62 recites. Asakawa and Tsu also fail to teach or suggest a buried conductive structure within a monocrystalline substrate, the conductive structure "forming at least a part of an interconnect between devices" and "being *completely surrounded* by monocrystalline material," as in the claimed invention (emphasis added). For at least these reasons, the Office Action fails to establish a *prima facie* case of

obviousness and withdrawal of the rejection of claims 62-64 and 67-71 is respectfully requested.

Claims 65, 74 and 80 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asakawa in view of Tsu and Kenney. Applicants note that, as described above, the cited prior art references, whether considered alone or in combination, fail to teach or suggest all limitations of independent 62, 72 and 76. Accordingly, withdrawal of the rejection of dependent claims 65, 74 and 80 is also respectfully requested.

Claims 76-79 and 81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (U.S. Patent No. 5,963,838) ("Yamamoto") in view of Bai et al. (U.S. Patent No. 5,861,340) ("Bai") and further in view of Kenney. This rejection is respectfully traversed.

As noted above, amended independent claim 76 recites an "integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline material of a same conductivity type of said monocystalline substrate." Amended independent claim 76 also recites that the first and second buried conductive patterns form "at least a part of first and second interconnects between devices, respectively, wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate."

Yamamoto relates to a "transistor element . . . formed on the surface of a silicon substrate." (Abstract). According to Yamamoto, "[a] tunnel is formed in the

silicon substrate at a position right under the transistor element" and "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). Yamamoto also teaches that "[s]ilicon oxide films are respectively formed on the inner surfaces of the tunnel and the contact hole" and that "[a] wiring layer is buried in the tunnel and the contact hole." (Abstract).

Bai relates to a "method of forming a polycide thin film." (Abstract). Bai teaches that "[F]irst, a silicon layer is formed" and that "[N]ext, a thin barrier layer is formed on the first silicon layer." (Abstract). According to Bai, "[A] second silicon layer is then formed on the barrier layer" and "a metal layer is formed on the second silicon layer." (Abstract). In this manner, "[T]he metal layer and the second silicon layer are then reacted together to form a silicide." (Abstract).

The subject matter of claims 76-79 and 81 would not have been obvious over Yamamoto in view of Bai and Kenney, whether considered alone or in combination. Specifically, the October 19, 2005 Office Action fails to establish a *prima facie* case of obviousness. None of Yamamoto, Bai or Kenney, alone or in combination, discloses, teaches or suggests all limitations of independent claim 76. Yamamoto does not disclose, teach or suggest "buried conductor patterns . . . completely surrounded by the same monocrystalline material of a same conductivity type," as independent claim 76 recites. In Yamamoto, wiring layer 32, which would arguably correspond to the "buried conductor pattern" of the claimed invention, is surrounded by substrate 21, well 25 and conductive film 37, and is not "completely surrounded by the same monocrystalline material of a same conductivity type," as in the claimed invention.

Similarly, Bai is silent about a buried conductor pattern, much less about a "buried conductor pattern" "forming at least a part of an interconnect between devices," or about a "buried conductor pattern . . . being completely surrounded by

monocrystalline material," as in the claimed invention (emphasis added). Kenney also fails to disclose, teach or suggest any of the limitations of claim 76. Kenney teaches a "process for forming a horizontal trench exclusively in heavily doped p+ regions is presented in which porous silicon is first formed in the p+ regions and then the porous silicon is etched," and not "buried conductor patterns . . . completely surrounded by the same monocrystalline material of a same conductivity type," as independent claim 76 recites.

Applicants further note that, to establish a *prima facie* case of obviousness, "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573. This way, a rejection of a claim for obviousness in view of a combination of prior art references must be based on a showing of a suggestion, teaching, or motivation that has to be "clear and particular." In re Dembiczak, 175 F.3d at 999. Thus, the mere fact that it is possible to find two isolated disclosures which might be combined to produce a new compound does not necessarily render such production obvious, unless the prior art also suggests the desirability of the proposed combination.

The October 19, 2005 Office Action fails to establish a *prima facie* case of obviousness because, as the Court in Northern Telecom, Inc. noted, "[i]t is insufficient

that the prior art disclosed the components of the patented device" and there is no "teaching, suggestion, or incentive to make the combination." Northern Telecom, Inc., 908 F.2d at 934. On one hand, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). For this, Yamamoto teaches that "[a] tunnel is formed in the silicon substrate at a position right under the transistor element" and that "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). On the other hand, the crux of Bai is a method of forming a polycide film with increased thermal stability. For this, Bai teaches that a plurality of layers are formed over a substrate as part of a gate electrode and subjected to various thermal conditions. Thus, Yamamoto and Bai do not even have in common the substrate on which their respective structures are formed. In addition, a person of ordinary skill in the art would not have been motivated to combine Yamamoto, which teaches the formation of wiring layers *below* a surface of a substrate, with Bai, which teaches the formation of a thin silicide layer *over* a surface of a substrate.

For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 76-79 and 81 is respectfully requested.

Allowance of the application is solicited.

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Respectfully submitted,

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